SPLIT POLY-SiGe/POLY-Si ALLOY GATE STACK

Abstract of the Disclosure

A multi-layered gate electrode stack structure of a field effect transistor device is formed on a silicon nano crystal seed layer on the gate dielectric. The small grain size of the silicon nano crystal layer allows for deposition of a uniform and continuous layer of poly-SiGe with a [Ge] of up to at least 70% using in situ rapid thermal chemical vapor deposition (RTCVD). An in-situ purge of the deposition chamber in a oxygen ambient at rapidly reduced temperatures results in a thin SiO_2 or $Si_xGe_yO_z$ interfacial layer of 3 to 4A thick. The thin SiO_2 or $Si_xGe_yO_z$ interfacial layer is sufficiently thin and discontinuous to offer little resistance to gate current flow yet has sufficient [O] to effectively block upward Ge diffusion during heat treatment to thereby allow silicidation of the subsequently deposited layer of cobalt. The gate electrode stack structure is used for both nFETs and pFETs.